In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended.

1. (Previously Presented) An integrated circuit including

a first layer having metal or metal alloy at a surface thereof,

a second layer adjacent to said surface having a metal or metal alloy via therein,

an interlayer connection between metal or metal alloy of said first layer and said metal or metal alloy via comprising a stable alloy region having a concentration of alloying material which is continuously graded from a reaction front where a stoichiometric alloy has been formed and graded mechanical characteristics, containing a predetermined quantity of alloying material and restricted to an interfacial region of said metal or metal alloy of said first layer and said metal or metal alloy via by a barrier layer and by said quantity of alloying material being fully reacted with said metal or metal alloy of said first layer or said second layer.

2. (Original) The integrated circuit as recited in claim 1, wherein said metal or metal alloy of said first layer is a first metal and said metal or metal alloy of said second layer is a second metal.

3. (Original) The integrated circuit as recited in claim 1, wherein said metal or metal alloy comprises copper

4. (Original) The integrated circuit as recited in claim 1, wherein said barrier includes a layer of tantalum, tungsten or titanium or alloys or nitrides thereof.

5. (Original) The integrated circuit as recited in claim 1, wherein said barrier comprises a layer of tantalum nitride and a layer of tantalum.

6. (Original) The integrated circuit as recited in claim 1, wherein said metal alloy of said interlayer connection at said interface includes tin, indium, nickel, gold, silver, aluminum, beryllium, tellurium, magnesium, zinc or zirconium.

7. (Original) The integrated circuit as recited in claim 1, wherein said barrier is above said interlayer connection and said metal alloy of said interlayer connection is confined to a region below said barrier.

8. (Currently Amended) The integrated circuit as recited in claim 1, wherein said metal alloy of said interlayer connection is formed as an annulus in said metal or metal alloy at a surface of said first layer.

9. (Original) The integrated circuit as recited in claim 8, wherein said via extends into said metal or metal alloy of said first layer surrounded by said annulus.

10. (Withdrawn) The integrated circuit as recited in claim 1, wherein said barrier is below said interlayer connection and said metal alloy of said interlayer connection is confined to a region above said barrier.

11. - 20. (Canceled)

21. (New) The integrated circuit as recited in claim 1, wherein said interfacial region extends approximately one diffusion length of said alloying material in said metal or metal alloy of said first layer or said second layer from said reaction front where said stoichiometric alloy has been formed.

22. (New) An integrated circuit including

a first layer having metal or metal alloy at a surface thereof,

a second layer adjacent to said surface having a metal or metal alloy via therein,

an interlayer connection between metal or metal alloy of said first layer and said metal or metal alloy via comprising a stable alloy region having graded mechanical characteristics, containing a predetermined quantity of alloying material and restricted to an interfacial region of said metal or metal alloy of said first layer and said metal or metal alloy via by a barrier layer,

wherein said metal alloy of said interlayer connection is formed as an annulus in said metal or metal alloy at a surface of said first layer.

23. (Currently Amended) The integrated circuit as recited in claim ~~21~~ 22, wherein said via extends into said metal or metal alloy of said first layer surrounded by said annulus.